



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,737	01/14/2000	Hansjorg Reichert	GR-97-P-1903	8769
24131	7590	03/27/2006	EXAMINER	
LERNER GREENBERG STEMER LLP P O BOX 2480 HOLLYWOOD, FL 33022-2480			SEFER, AHMED N	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

---

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

**MAILED**

**MAR 27 2006**

**GROUP 2800**

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 09/483,737  
Filing Date: January 14, 2000  
Appellant(s): REICHERT ET AL.

Laurence A. Greenberg  
For Appellant

### **EXAMINER'S ANSWER**

This is in response to the appeal brief filed 12/9/2005 appealing from the Office action mailed 9/9/2005.

#### **(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

#### **(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

#### **(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

#### **(4) Status of Amendments After Final**

No amendment after final has been filed.

#### **(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

#### **(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

#### **(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

#### **(8) Evidence Relied Upon**

Art Unit: 2826

WO 88/03705

Fister et al

5-1988

5,234,153

Bacon et al

8-1993

### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

#### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 6-326210) (of record) in view of Fister et al. ("Fister") WO 88/03705 and Bacon et al. ("Bacon") USPN 5,234,153.

Ishii discloses in fig. 2 a semiconductor component comprising a solder containing at least two components with at least two constituents including a first constituent containing a precious metal and a second constituent being consumed during a soldering operation by one of reacting and being dissolved in material which are to be joined; a substrate 40; a chip 1 having a rear side and a diffusion barrier 7a; said semiconductor chip being secured at said rear side to a substrate 40 by a solder containing gold and tin solder 8 and said solder having a hypereutectic concentration containing gold-tin (AuSn) with a hypereutectic Sn concentration and containing a gold-tin compound (AuSn) having a composition which falls within the range recited in the claim; and said a semiconductor chip being secured to said substrate by one of alloying and

Art Unit: 2826

brazing using said solder but lacks anticipation of an adhesive or diffusion barrier provided on said rear side of semiconductor chip or solder thickness.

Fister discloses in figs. 1-5 a semiconductor component comprising a solder 18 containing at least two components with at least two constituents including a first constituent containing a precious metal and a second constituent; a substrate 14; and a semiconductor chip 12 having a rear side and adhesive 19 provided on said rear side; and said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form chip-substrate connection by said solder.

Bacon teaches (see col. 1 lines 50-63 and claim 7) the advantage of using a thin gold-tin compound solder.

Since Ishii, Fister and Bacon are all from the same field of endeavor, semiconductor die attach system, the teachings of Fister and Bacon would have been recognized in Ishii's pertinent art. Therefore, in view of Fister's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Ishii's device by incorporating an adhesive on a rear side of a semiconductor chip since that would dissipate thermal cycling stresses as taught by Fister. It would have been obvious to incorporate a thin solder, since that would provide a better thermal conductance as taught by Bacon.

#### **(10) Response to Argument**

The appellants argue that the combined references listed above do not disclose all of the elements of the device structure as recited in the claim. Specifically, The appellants argue that the cited references disclose neither an adhesive provided on a rear side of a semiconductor chip nor forming a chip-substrate connection by a solder.

Art Unit: 2826

The examiner respectfully disagrees with the appellants because:

Ishii discloses the device structure as recited in the claim. What Ishii lacks, an adhesive provided on a rear side of a semiconductor chip and forming a chip-substrate connection by a solder, is taught by Fister which discloses an adhesive 19 provided on a rear side of a semiconductor chip 12 and forming a chip-substrate connection by a solder 18 -- Note that the claim language does not exclude a buffer layer between an adhesive/diffusion barrier and a solder. Furthermore, Bacon teaches the advantages of a thin -- less than 4 $\mu$ m -- gold-tin solder.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

ANS *ANS*  
*by [signature]*

February 28, 2006

*[Signature]*  
NATHAN FLYNN  
SENIOR PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Conferees:

Nathan Flynn *NF*

Darren Schuberg *DS*